

LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A test circuit for a semiconductor integrated circuit device for being put to a delay test using a scan path test circuit incorporated on said semiconductor integrated circuit device for a scan path test, comprising:

a two-pulse generator for generating two pulses spaced from each other by a pulse interval equal to a period of a test clock for the delay test, said test clock being ~~input from an external source, from said test clock,~~ and supplying the generated two pulses to the scan path test circuit, said two-pulse generator comprises a gate signal generator for generating a gate signal to extract two pulses from said test clock and a latch gate circuit for outputting two pulses from said test clock according to said gate signal, said gate signal generator generating one of a positive and negative edge of said gate signal at ~~after~~ a predetermined ~~interval~~ time delay after ~~[[an]]~~ a negative edge of said test clock as measured from an input timing of a control signal.

2. (Previously Presented) The test circuit according to claim 1, wherein said test circuit is fabricated in said semiconductor integrated circuit device and further comprises:

a PLL circuit for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator.

3. (Previously Presented) The test circuit according to claim 1, wherein said test circuit is mounted on a test board, and said semiconductor integrated circuit device is removably mounted on said test board.

4. (Previously Presented) The test circuit according to claim 3, further comprising: a PLL circuit for multiplying the frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator.

5. (Withdrawn) A device for testing a semiconductor integrated circuit device for being put to a delay test using a scan path test circuit incorporated in the semiconductor integrated circuit device for a scan path test, comprising:

a test board on which a semiconductor integrated circuit device to be tested is removably mounted; and

a two-pulse generator mounted on said test board, for generating two pulses spaced from each other by a pulse interval equal to a period of a test clock for the delay test, from said test clock, and supplying the generated two pulses to the scan path test circuit.

6. (Withdrawn) A device according to claim 5, further comprising: a PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator.

7. (Withdrawn) A device according to claim 5, further comprising: a clock generator for outputting said test clock.

8. (Withdrawn) A device according to claim 6, further comprising: a clock generator for outputting said test clock.

9. (Withdrawn) A device according to claim 5, said two-pulse generator comprises: a gate signal generator for generating a gate signal to extract two pulses from said test clock; and a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

10. (Withdrawn) A device according to claim 6, said two-pulse generator comprises: a gate signal generator for generating a gate signal to extract two pulses from said test clock; and a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

11. (Withdrawn) A device according to claim 7, said two-pulse generator comprises: a gate signal generator for generating a gate signal to extract two pulses from said test clock; and a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

12. (Withdrawn) A device according to claim 8, said two-pulse generator comprises: a gate signal generator for generating a gate signal to extract two pulses from said test clock; and a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

13. (Withdrawn) A device according to 5, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

14. (Withdrawn) A device according to 6, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

15. (Withdrawn) A device according to 7, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

16. (Withdrawn) A device according to 8, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

17. (Withdrawn) A device according to 9, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

18. (Withdrawn) A device according to 10, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

19. (Withdrawn) A device according to 11, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

20. (Withdrawn) A device according to 12, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

21. (Previously Presented) The test circuit according to claim 3, further comprising: a clock generator for outputting said test clock. a test board on which a semiconductor integrated circuit device is removably mounted.

22. (Previously Presented) The test circuit according to claim 3, further comprising: a frequency divider mounted on said test board, for dividing the frequency of said test clock into a lower frequency.

23. (Previously Presented) The test circuit according to claim 1, further comprising: a clock generator for outputting said test clock, wherein said two-pulse generator is fabricated in said semiconductor integrated circuit device, and said semiconductor integrated circuit device is removably mounted to a test board, and said clock generator is mounted on said test board.

24. (Previously Presented) The test circuit according to claim 23, further comprising: a PLL circuit for multiplying the frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator, wherein said PLL circuit is fabricated in said semiconductor integrated circuit device.

25. (Withdrawn) A device according to claim 21, further comprising: a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

26. (Withdrawn) A device according to claim 22, further comprising: a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

27. (Withdrawn) A device according to claim 23, further comprising: a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

28. (Withdrawn) A device according to claim 24, further comprising: a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

29. (Withdrawn) A device according to claim 21, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

30. (Previously Presented) The test circuit according to claim 23, further comprising: a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

31. (Withdrawn) A device according to claim 23, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

32. (Previously Presented) The test circuit according to claim 23, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a lower frequency.

33. (Withdrawn) A device according to claim 25, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

34. (Withdrawn) A device according to claim 26, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

35. (Withdrawn) A device according to claim 27, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

36. (Withdrawn) A device according to claim 28, further comprising: a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

37. (Previously Presented) The test circuit according to claim 1, wherein said gate signal generator comprises a control circuit for adjusting a timing of said gate signal.

38. (Previously Presented) The test circuit according to claim 37, wherein said control circuit counts said test clock for adjusting said timing of said gate signal.